ASPL-FPGA IO- 0A

FPGA-Based Scalable Digital I/O Module

Ver 1.0/2018

PRODUCT DATASHEET

Atindriya's FPGA-based Digital I/O Module (ASPLFPGA IO-0A) is a standardized, high-density digital I/O building block designed for large Automated Test Equipment (ATE) platforms requiring thousands of deterministic I/O lines. Developed with a fully indigenous FPGA architecture and proven in multiple defence test systems supplied to DRDO Labs (CABS, LRDE etc) , the module enables linear scalability from hundreds to few thousands digital I/O lines by simple replication, without any change to the base hardware design. With fixed interfaces, configurable firmware, and distributed control architecture, the solution offers a robust, long-term alternative to proprietary I/O cards for radar, avionics, EW, and missile test applications.

Features

- High-speed serial LVDS control interface
- Local serial-to-parallel decoding
- Reduced cabling and lower BOM cost
- Fast inter-module switching
- Parallel operation across multiple modules
- Scalable and modular design

Key Parameters	
FPGA Part Number	***XC7A200T-1FFG1156I – AMD- Xilinx***
Logic Cells	***215,360***
Block RAM	***13,455,360 bits***
Configuration Flash	***256Mb –QSPI Memory***
User I/O pins	***400(TTL I/O's)***
LVDS interface	***10 no's***
RS422 interface	***5 no's***

Environmental:

- Temperature: -20^{0}C to +55^0 C
- Storage Temperature: -40^{0}C to + 85^0

Outline Drawing:

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This device provides sufficient logic resources, high-speed I/O capability, and deterministic performance required for real-time control and parallel signal distribution.

The FPGA I/O Module is a distributed control module designed for high-speed, low-latency I/O control applications. The module minimizes cabling and system cost by utilizing high-speed serial LVDS interfaces.

Interfaces

RS-232 : 1 port

RS-422 : 1 port

LVDS : 10 differential pairs

TTL I/Os : 400

SL NO	*PARAMETER*	*SPECIFICATIONS*
1	*Model no*	*ASPLFPGA IO-0A*
2	*FPGA Part Number*	*XC7A200T-1FFG1156I – AMD- Xilinx*
3	*Logic Cells*	*215,360*
4	*Block RAM*	*13,455,360 bits*
5	*Configuration Flash*	*256Mb –QSPI Memory*
6	*User I/O pins*	*400(TTL I/O's)*
7	*LVDS Pairs*	*10 no's*
8	*Operating Temperature*	-20°C to +55°C
9	*Connector Type*	D Type / Circular
10	*9-pin Debug connector*	J-Tag ,RS232 ,RS422 ports
11	*Unit Dimensions **	L*W*H(120*120*60mm)
		*Varies with connector type and Mounting Structure

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Previous Projects / Subsystems employed this IO Module:

Project: MySIR Test RIG
End Customer: CABS – DRDO
Purpose : To control 0.5-18GHz Co-Axial Switches in RWR Switch Matrix

Project: AEW&C Primary Radar Testing
Customer: LRDE – DRDO and CABS - DRDO
Purpose : To control 32 Channel 6-bit Phase Shifter and 32 Channel 6-Bit Attenuator

Parameters are subject to change. For more information:

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